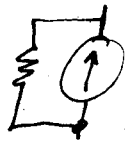
NOISE IN MOSFETS

1. Thermal Noise
2. $\frac{1}{f}$ or flicker noise

1. Thermal noise

- Generated by parasitic resistances at
  - drain (R_D)
  - source (R_S)
  - gate (R_G)
- For each R, add noise source



$$\sqrt{\overline{i_R^2}} = \sqrt{\frac{4kT}{R}}$$

- DOMINANT SOURCE IS thermal noise from channel

Sat $\overline{i_{th}^2} = 4kT\gamma g_m$ where $\gamma = \begin{cases} \frac{2}{3} & \text{long channel} \\ 2.5 & 0.25\,\mu m \text{ FETS} \end{cases}$

TRIODE $\overline{i_{th}^2} = \frac{4kT}{R_{on}} = 4kTg_m \quad (\gamma = 1)$

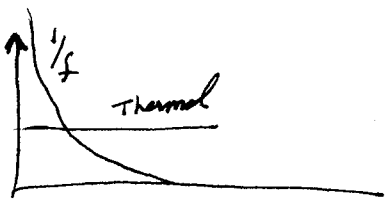
2. Flicker or 1/f noise

- Electrons trapped & detrapped at Si/SiO_2 interface
  $\Rightarrow \Delta I_D$ due to R-G to & from trap states.

$\tau_{R\text{-}G} \sim \mu s$

$S_i(f) \sim \frac{1}{f}$

Falls off at high frequencies.



- SPICE Model (NLEV = 0)

$$\sqrt{\overline{i_{1/f}^2}} = \sqrt{\frac{KF \cdot I_D^{AF}}{(C_{ox}' \cdot L)^2 f}}$$

KF = flicker noise coefficient $\sim 10^{-30}$ A^{2-AF} $\left(\frac{F}{m^2}\right)$

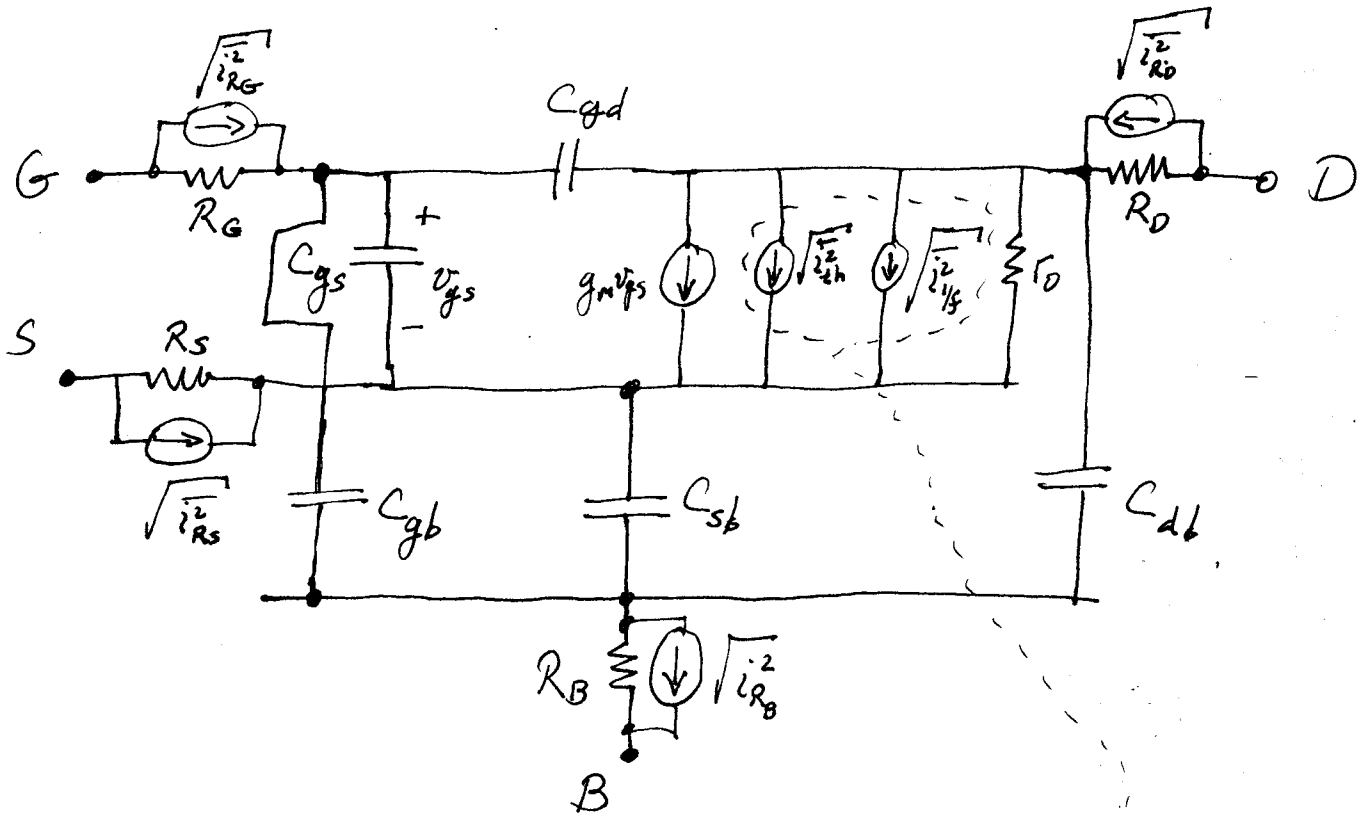
$I_D = I_D$ (DC drain current)

AF = flicker noise exponent (0.5 – 2)

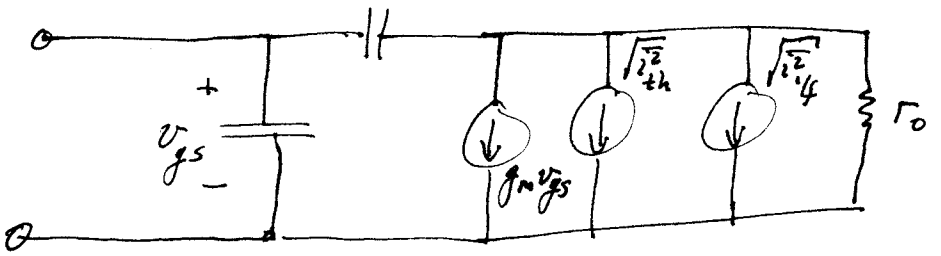
f = frequency

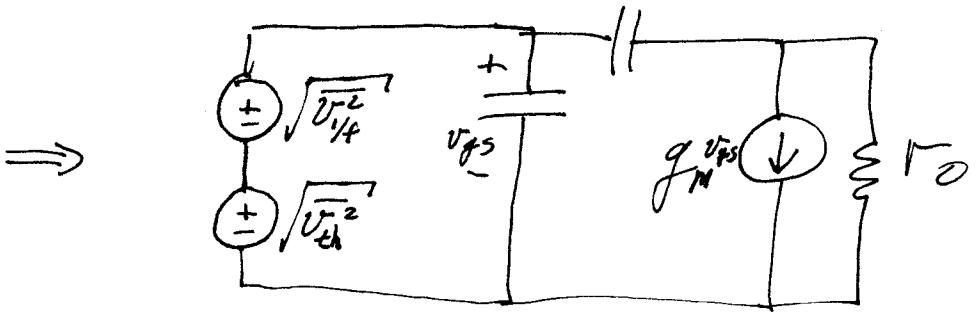
- SPICE MODEL (NLEV = 1)

$$\sqrt{\overline{i^2_{1/f}}} = \sqrt{\frac{KF \cdot I_D^{AF}}{C_{ox}^{-2} WL\, f}}$$



- Dominant sources from channel -
For hand calculations ignore rest.





$$\sqrt{\overline{v_{th}^2}} = \frac{\sqrt{\overline{i_{th}^2}}}{g_m}$$

$$\sqrt{\overline{v_{1/f}^2}} = \frac{\sqrt{\overline{i_{1/f}^2}}}{g_m}$$

NOTE:

Small signal (analog) model is a LINEAR model → Noise calculation goes exactly as before.

GOAL: OP-AMP CH. 25

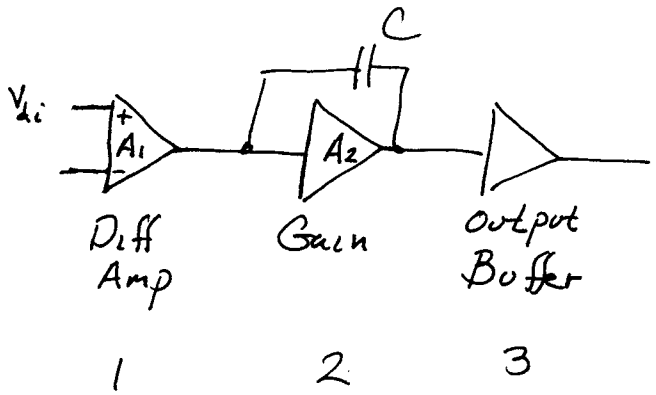
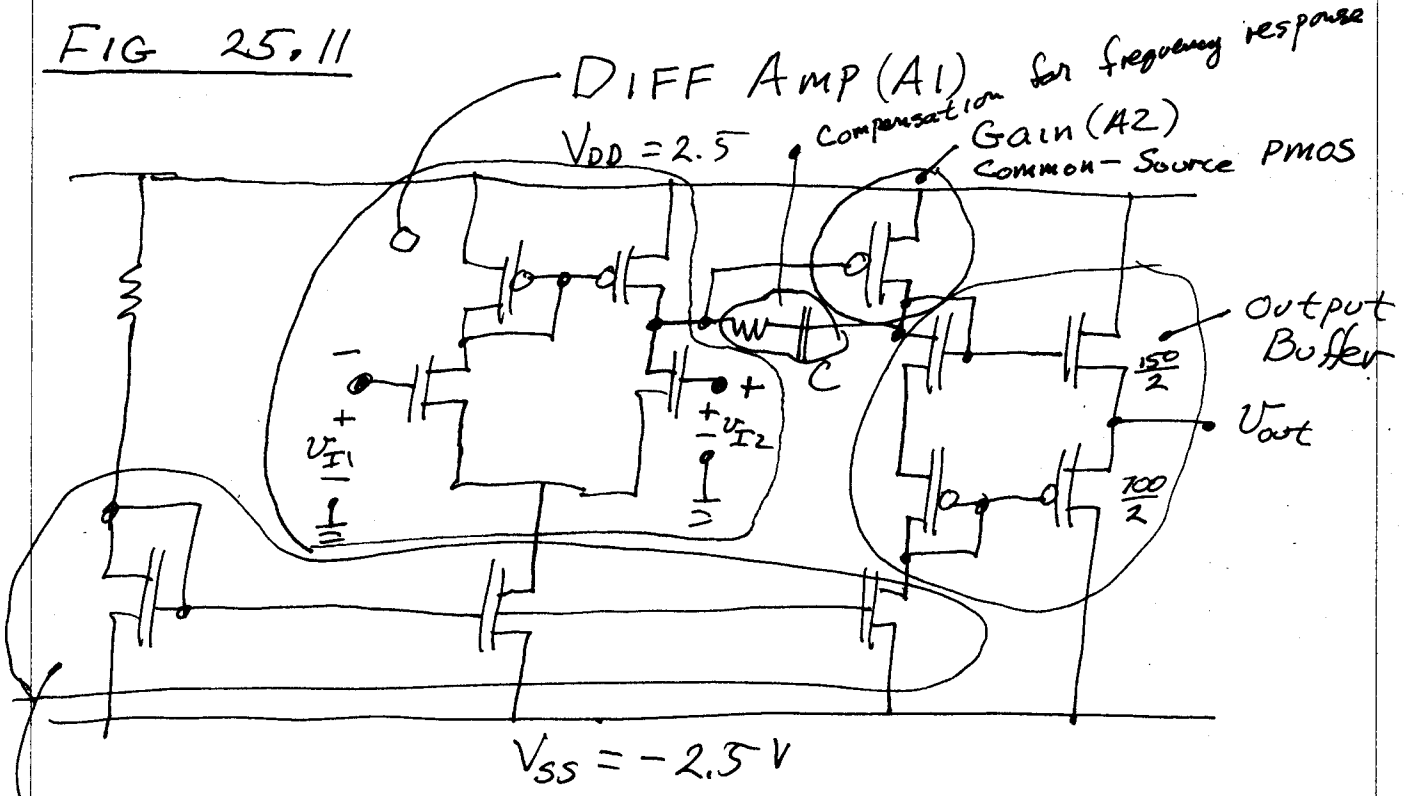


FIG 25.11

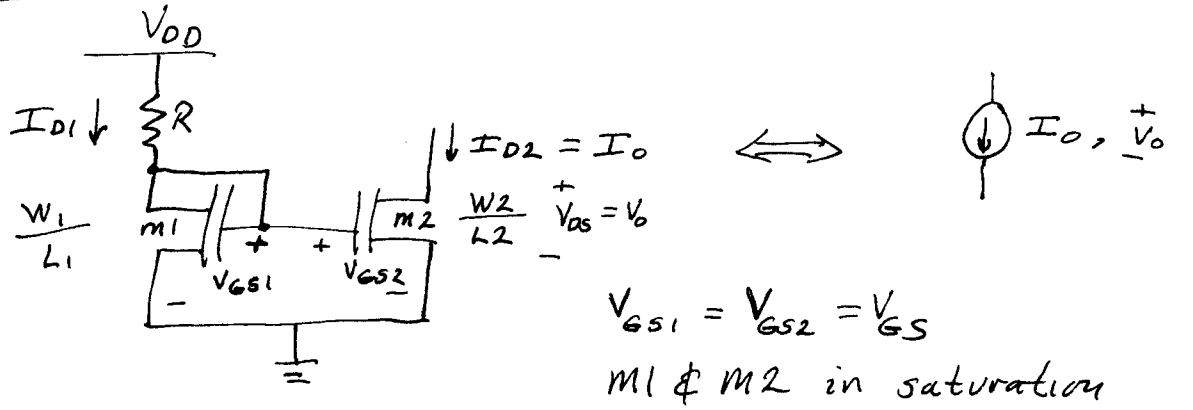


Current Mirror for DC biasing
Current Mirrors CH. 20

Current Sources & Sinks Ch. 20

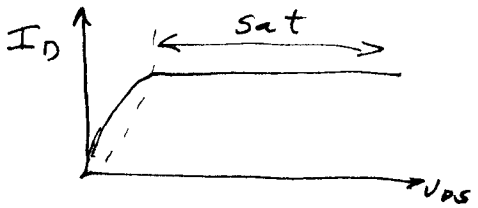
Current Mirror

Current sink (NMOS)



$V_{GS1} = V_{GS2} = V_{GS}$

M1 & M2 in saturation



BASIC EQUATIONS

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{TH})^2$$

$$I_{D2} = \frac{\beta_2}{2}(V_{GS} - V_{TH})^2$$

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2/L_2}{W_1/L_1} = \frac{W_2 L_1}{W_1 L_2}$$

$$I_{D1} = \frac{V_{DD} - V_{GS}}{R} = \frac{\beta_1}{2}(V_{GS} - V_{TH})^2$$

$\Rightarrow$ Solve Quadratic Eq^n for V_{GS}

~~DESIGN~~

IDEAL Current source has ∞ output R.

$$r_{O2} = \frac{1}{\lambda I_{O2}} = \text{BIG}$$

DESIGN VARIABLES

L_1, W_1, L_2, W_2, V_{GS}

- Keep r_{O2} as high as possible

$\Rightarrow$ choose $L_2 \sim$ 2–5 × minimum L

– reduces channel length modulation
high field effects
DIBL

Choose $L_1 = L_2$.

• V_{GS}: (i) choose so that you stay in saturation

$V_{DS} > V_{GS} - V_{TH} \Leftrightarrow$ sets upper limit

(ii) $I_{D2} = \frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2} (V_{GS} - V_{TH})^2$

For V_{GS} approaching V_{TH}, need BIG W_2 to get enough current.

Rule of thumb: choose $V_{GS} \sim 200^{-500}$ mV $> V_{TH}$.

$\Rightarrow \frac{I_{D2}}{I_{D1}} = \frac{W_2}{W_1}$ only design vars. left.

EG: Design $I_{D2} = 10\mu A$ w/ $V_{DD} = 5V$ (CN20 process)

1) Choose $V_{GS} =$ ~~10 mA~~ ~~2.5 V~~ 1.2 V

2) Choose $L_1 = L_2 = 5\mu m$

3) Find R: (assume $I_{D1} = I_{D2} = 10\mu A$) $\Leftrightarrow W_1 = W_2$

$$R = \frac{V_{DD} - V_{GS}}{I_{D1}} = \frac{5 - 1.2\,(V)}{10\,e{-}3\,(mA)} = 380\,k\Omega$$

4) $I_{D1} = I_{D2} = 10\mu A = \frac{KP_n}{2} \frac{W}{L} (V_{GS} - V_{THN})^2$

$$= \frac{50 \frac{\mu A}{V^2}}{2} \frac{W}{5\mu m} (1.2 - 0.83)^2 \Leftrightarrow W_1 = W_2 = 14.61\,\mu m \rightarrow 15\,\mu m$$

BIASING REQUIREMENT

TO Keep M2 in saturation:

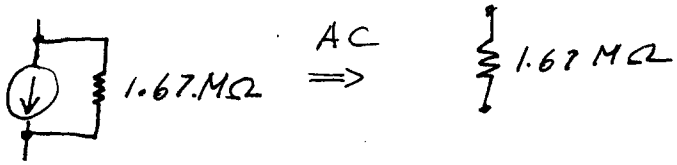
$$V_{DS2} > V_{GS} - V_{THN} = 1.2 - 0.83 = \underline{0.37\ V}$$

$V_{DS2} > 0.37\ V$ (excess gate voltage)

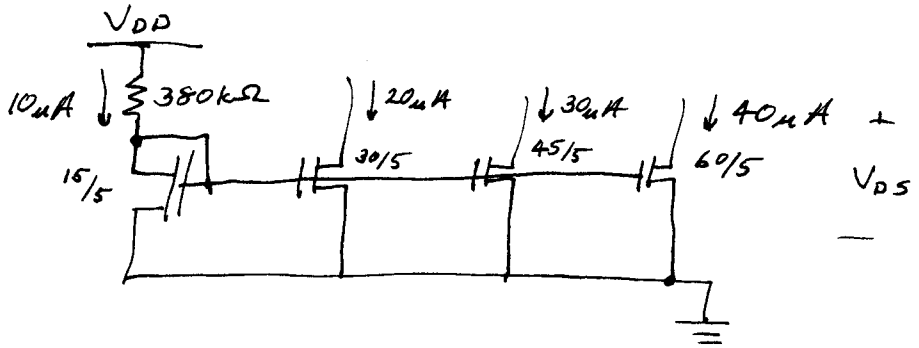
Output resistance

$$r_o = \frac{1}{\lambda I_o} = \frac{1}{0.06 \times 10e\text{-}3mA} = 1.67\ M\Omega$$

Low f AC small signal Analysis:



Multiple Mirrors



$V_{DS} > 0.37\ V$

CURRENT SOURCES (PMOS)