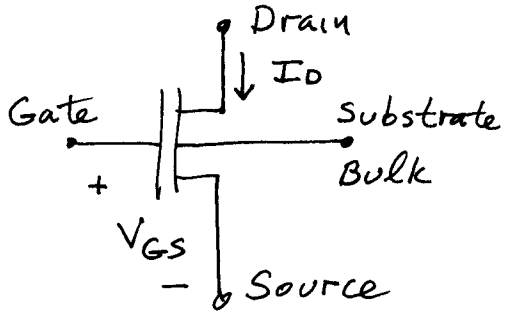
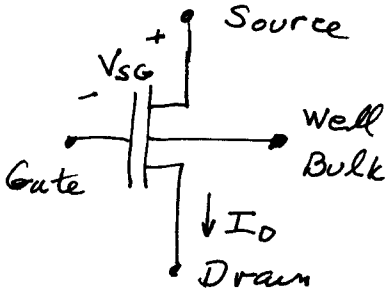
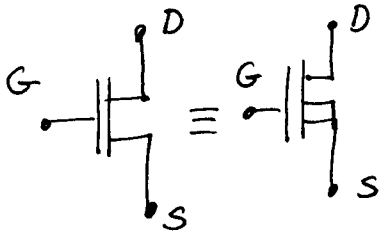
CH 5. MOSFET (Review)

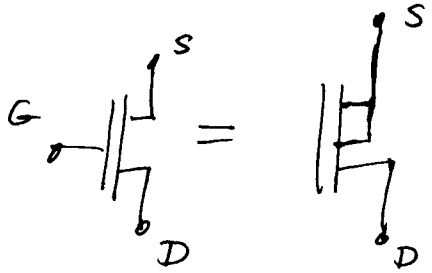
NMOS



PMOS



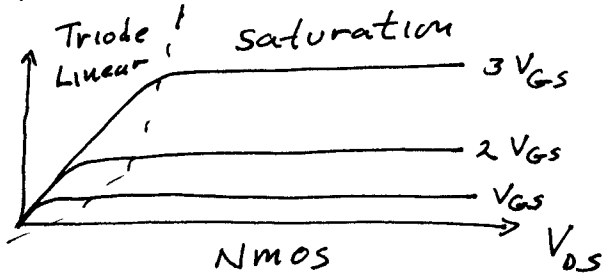




MOSFET I-V

GRADUAL Channel Approximation

Square law



TRIODE REGION

NMOS ($V_{GS} \geq V_{THN}$ & $V_{DS} < V_{GS} - V_{THN}$)

$$I_D = \underbrace{\mu_n C'_{ox}}_{KP_n} \frac{W}{L}\left[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

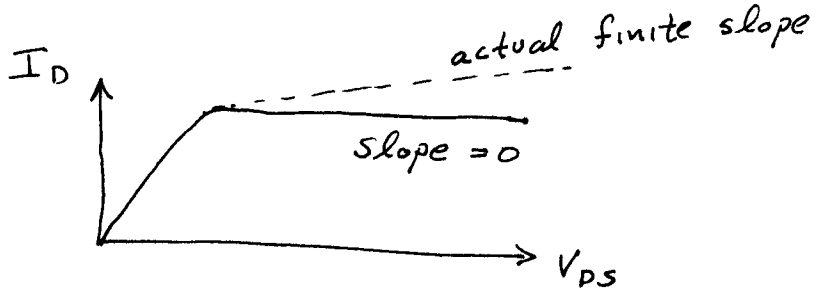
PMOS ($V_{SG} \geq V_{THP}$ & $V_{SD} < V_{SG} - V_{THP}$)

$$I_D = \underbrace{\mu_p C_{ox}}_{KP_p} \frac{W}{L}\left[(V_{SG} - V_{THP})V_{SD} - \frac{V_{SD}^2}{2}\right]$$

Saturation

NMOS ($V_{GS} \geq V_{THN}$ & $V_{DS} \geq V_{GS} - V_{THN}$)

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{THN})^2$$



Finite slope from channel length modulation

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{THN})^2\left[1 + \lambda_c(V_{DS} - V_{DS,sat})\right]$$

↑ channel length modulation parameter.

PMOS ($V_{SG} \geq V_{THP}$ & $V_{SD} > V_{SG} - V_{THP}$)

$$I_D = \frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{SG} - V_{THP})^2\left[1 + \lambda_c(V_{SD} - V_{SD,sat})\right]$$

6.2.3 Subthreshold (Weak inversion)

($V_{GS} < V_{THN}$ ~~100mV & $V_{DS} > 100mV$~~)

$$I_D = \mu_n C_{ox}' \frac{W}{L} \left(\frac{k_B T}{q}\right)^2 e^{1.8} e^{q(V_{GS}-V_{THN})/(N' \cdot k_B T)} \cdot \left[1 - e^{-q V_{DS}/kT}\right]$$

$(N' = N0' - NB' \cdot V_{SB} + ND' \cdot V_{DS})$ (6.27)

For $V_{DS} > \frac{3kT}{q}$,

$$I_D = I_{DO} e^{q(V_{GS}-V_{THN})/(N' \cdot kT)}$$

$$I_{DO} = \mu_n C_{ox}' \frac{W}{L} \left(\frac{kT}{q}\right)^2 e^{1.8}$$

Subthreshold Slope

$$\log_{10} I_D = \log I_{DO} + \frac{q(V_{GS}-V_{THN})}{N' \cdot kT} \cdot \log e$$

$$\frac{d \log_{10} I_D}{d V_{GS}} = \frac{q}{N' kT} \log_{10} e$$

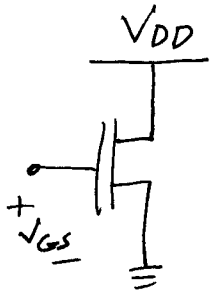
Inverse is common figure of merit:

$$\left(\frac{d \log_{10} I_D}{d V_{GS}}\right)^{-1} = \frac{N' kT}{q} \frac{1}{\log_{10} e}$$

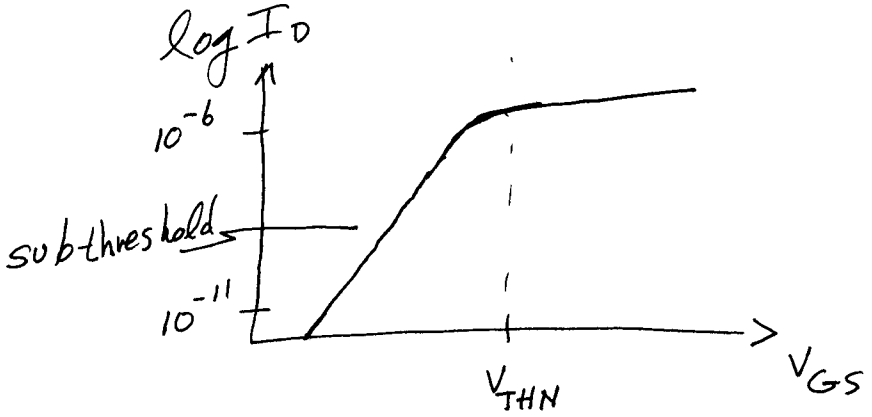
Ideal: $N' = 1$

$$\boxed{\left(\frac{d \log_{10} I_D}{d V_{GS}}\right)^{-1} = 60 \text{ mV/decade}}$$

Subthreshold slope of $60 \frac{mV}{decade}$ is ideal. Standard of comparison. Measure of how well a FET turns off in digital applications.



The larger the subthreshold slope, the slower the current shuts off.



Subtheshold slope tells you how many mV of gate voltage it takes to reduce I_D by a factor of 10.

This has become one of THE primary concerns for ultra-scaled FETs.

As $L \downarrow$, can't shut device off.

SPICE (Simulation Program with Integrated Circuit Emphasis)

Flavors

Berkeley SPICE The original SPICE. Open source. Download from Berkeley web site

HSPICE Now owned by Synopsis. The industrial standard. UNIX based.

SPECTRE Cadence. Improved Berkeley SPICE. Supports all models UNIX

PSPICE Windows. Support all models.

TRANSISTOR (MOSFET) MODELS

	SPICE	HSPICE
Level 1-3	first generation models	
BSIM 1	Level 4	Level 28 (or 13?)
BSIM 2		Level 39
BSIM 3V3	Level 8	49 (3V2 = Level 47)
BSIM 4	Level 14	Released 2000.

De facto industry standard.
Level 1 = Long channel "textbook" model.

Ch. 6 BSIM SPICE MODEL

BSIM (Berkeley Short Channel IGFET Model)

IGFET (Insulated Gate FET)

Fabs supply a BSIM3 model for their process.

BSIM 3 model documentation (class web page)

ANALOG MOSFET MODEL CH. 9

Small Signal Frequency dependent