Digital Integrated Circuit (IC) Layout and Design - Week 4, Lecture 8

- http://www.ee.ucr.edu/~rlake/EE134.html
- HW 1 due next Tues.
Reading

- Week 1 - Read Chapter 1 of text.
- Week 2 - Read Chapter 2 of text.
- Week 3 - Read Chapter 3 of text.
- Week 4 - Read Chapter 5 of text.
Review/Finish

- Inverter (Ch. 5)
  - Voltage transfer curve (VTC)
  - Switching Point

New

- Inverter (Ch. 5)
  - Capacitance
  - Switching delay time
Simple Model versus SPICE

- $V_{DS} = V_{DSAT}$
- $V_{DS} = V_{GT}$

Diagram showing the relationship between $V_{DS}$ (V) and $I_D$ (A) with different regions labeled as Linear, Saturated, and Velocity Saturated.
A Unified Model for Manual Analysis

\[ V_{GT} = V_{GS} - V_T \]

for \( V_{GT} \leq 0 \): \( I_D = 0 \)

for \( V_{GT} \geq 0 \):

\[ I_D = k' \cdot \frac{W}{L} \cdot \left( V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS}) \]

with \( V_{min} = \min (V_{GT}, V_{DS}, V_{DSAT}) \)
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

<table>
<thead>
<tr>
<th></th>
<th>$V_{th}$ (V)</th>
<th>$\gamma$ (V$^{0.5}$)</th>
<th>$V_{DSAT}$ (V)</th>
<th>$k'$ (A/V$^2$)</th>
<th>$\lambda$ (V$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>$115 \times 10^{-6}$</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-30 \times 10^{-6}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

I keep all signs positive for PMOS and use $V_{SG}$, $V_{SD}$, $I_{SD}$. 
Voltage Transfer Characteristic
CMOS Inverter Load Characteristics

$V_{in} = 0$
$V_{in} = 0.5$
$V_{in} = 1$
$V_{in} = 1.5$
$V_{in} = 2$
$V_{in} = 2.5$

$V_{out}$

$I_{Dn}$

PMOS

NMOS
CMOS Inverter VTC

$V_{out}$

$V_{in}$

NMOS off
PMOS res
NMOS sat
PMOS res
NMOS res
PMOS sat
NMOS res
PMOS off

0.5 1 1.5 2 2.5

0.5 1 1.5 2 2.5
Switching Threshold as a function of Transistor Ratio

![Graph showing the relationship between switching threshold and transistor ratio. The graph plots $V_M$ (V) against $W_p/W_n$. The y-axis ranges from 0.8 to 1.8, and the x-axis ranges from $10^0$ to $10^1$. The line on the graph is upward-sloping, indicating an increase in switching threshold with increasing transistor ratio. There is a mathematical expression $= 0$ which likely represents a condition or equation related to the graph.](image-url)
Determining $V_{IH}$ and $V_{IL}$

A simplified approach

\[ V_{IH} - V_{IL} = \frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g} \]

\[ V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g} \]

\[ NM_H = V_{DD} - V_{IH} \quad NM_L = V_{IL} \]
Inverter Gain

\[ g = \frac{1}{I_D(V_M)} \left( \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p} \right) \]

\[ \approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)} \]
Gain as a function of VDD
Impact of Process Variations

The diagram illustrates the impact of process variations on the voltage transfer characteristic of a MOSFET inverter. The curves represent different transistor types and conditions:

- **Good PMOS**
- **Bad NMOS**
- **Good NMOS**
- **Bad PMOS**

The x-axis represents the input voltage ($V_{in}$) and the y-axis represents the output voltage ($V_{out}$). The curves are labeled as 'Nominal' indicating the ideal performance under normal process conditions.
CMOS Inverter
First-Order DC Analysis

\[ V_{in} = V_{DD} \]

\[ V_{in} = 0 \]

\[ V_{OL} = 0 \]
\[ V_{OH} = V_{DD} \]
\[ V_M = f(R_n, R_p) \]
CMOS Inverter: Transient Response

\[ t_{pHL} = f(R_{on}.C_L) = 0.69 \ R_n \ C_L \]

(a) Low-to-high

(b) High-to-low